In the Claims:

1. (Currently Amended) A method of manufacturing on a substrate a 2-transistor memory cell comprising a storage transistor having a memory gate stack and a selecting transistor, there being a tunnel dielectric layer between the substrate and the memory gate stack, the method comprising:

forming the memory gate stack by

providing a first conductive layer on the tunnel dielectric layer and a second conductive layer with a deposited interlayer dielectric layer between the first and second conductive layers, the deposited interlayer dielectric layer including oxide and being susceptible to undesirable growth upon exposure to oxygen during subsequent oxidation steps, ~~and~~

etching the second conductive layer thus forming a control gate, ~~and etching the first conductive layer thus forming a floating gate,~~

~~the method furthermore comprising,~~

~~before etching the first conductive layer,~~

forming spacers against the control gate in the direction of a channel to be formed under the tunnel dielectric layer, the spacers being formed from a dielectric material having an oxygen diffusion through the dielectric material that is, relative to oxide spacers, an order of magnitude smaller than oxygen diffusion through the oxide spacers, and

thereafter using the spacers as a hard mask to etch the first conductive layer thus forming the floating gate, the etching of the first conductive layer being an anisotropic dry etch that is selective to the tunnel dielectric, thereby using the tunnel dielectric to protect portions of the substrate laterally adjacent to the floating gate;

removing a portion of the tunnel dielectric laterally adjacent to the floating gate and exposing a portion of the substrate where the tunnel dielectric has been removed; and

forming an access gate dielectric oxide on the exposed portion of the substrate, using the spacers to mitigate the diffusion of oxygen to the deposited interlayer dielectric layer.

2. (Cancelled).

3. (Previously presented) A method according to claim 1, wherein the dielectric material having an oxygen diffusion through the material that is an order of magnitude smaller than oxygen diffusion through oxide spacers includes one or more of silicon nitride, silicon carbide or metal oxide.

4. (Previously presented) A method according to claim 1, furthermore comprising,

before forming the memory gate stack, applying the tunnel dielectric layer on the substrate, and

after formation of the memory gate stack, removing the tunnel dielectric layer by a selective etching technique at least at a location where the selecting transistor is to be formed, the selective etching technique preferentially etching the tunnel dielectric layer compared to the substrate.

5. (Currently Amended) A method according to claim 1, further including forming ~~comprising,~~

~~after etching of the first conductive layer, providing~~ a floating gate dielectric next to the formed floating gate ~~and at the same time providing an~~ while forming the access gate dielectric.

6. (Currently Amended) A method according to claim 1, ~~the memory gate stack comprising an interlayer dielectric layer between the first conductive layer and the second conductive layer, the method~~ furthermore comprising

removing part of the interlayer dielectric layer after forming the control gate but before forming the spacers.

7. (Previously presented) A method according to claim 1 wherein ~~, the selecting transistor comprising an access gate, the method comprising~~

forming an access gate includes forming the access gate while the spacer at the access gate side is still present.

8. (Currently amended) A 2-transistor memory cell comprising,

a storage transistor and

a selecting transistor, the storage transistor comprising

a floating gate dielectric on a substrate,

a floating gate on the floating gate dielectric, ~~and~~

a deposited interlayer dielectric layer on the floating gate,

a control gate~~, wherein the control gate is~~ on the interlayer dielectric layer and being smaller than the floating gate, and

spacers ~~are present~~ next to the control gate~~, and the spacers are~~ and made from a dielectric material having an oxygen diffusion through the dielectric material that is an order of magnitude smaller than oxygen diffusion through oxide spacers and that mitigates oxygen diffusion to the interlayer dielectric layer.

9. (Cancelled).

10. (Currently amended) A memory cell according to claim 8, the selecting transistor comprising an access gate on an access gate dielectric on the substrate immediately adjacent to a wet-etched portion of the floating gate dielectric, a spacer being present between the control gate and the access gate and a floating gate sidewall dielectric ~~being~~ that is contiguous with the access gate dielectric and present between the floating gate and the access gate, wherein the spacer is thicker than the floating gate dielectric.

11. (Previously presented) An electronic device comprising a 2-transistor memory cell including,

a storage transistor and

a selecting transistor, the storage transistor comprising

a floating gate dielectric on a substrate,

a floating gate on the floating gate dielectric, ~~and~~

a deposited interlayer dielectric layer on the floating gate,

a control gate~~, wherein the control gate is~~ on the interlayer dielectric layer and being smaller than the floating gate, and

spacers ~~are present~~ next to the control gate~~, and the spacers are~~ and made from a dielectric material having an oxygen diffusion through the dielectric material that, relative to oxide spacers, is an order of magnitude smaller than the oxygen diffusion through the oxide spacers and that mitigates oxygen diffusion to the interlayer dielectric layer.

12. (Cancelled).

13. (Currently amended) The electronic device as recited in claim 11, wherein the selecting transistor includes,

an access gate on an access gate dielectric on the substrate immediately adjacent to a wet-etched portion of the floating gate dielectric,

a spacer being present between the control gate, and

~~the access gate and~~ a floating gate sidewall dielectric ~~being~~ that is contiguous with the access gate dielectric and present between the floating gate and the access gate, wherein the spacer is thicker than the floating gate dielectric.

14. (New) A method according to claim 1,

wherein removing a portion of the tunnel dielectric includes wet etching the tunnel dielectric to remove a portion of the tunnel dielectric laterally adjacent to the floating gate and expose a portion of the substrate surface where the tunnel dielectric has been wet etched, leaving the exposed surface of the substrate intact, and

further including forming an access gate of the selecting transistor on the access gate dielectric.